REMARKS

Claims 1-9 are pending in this application; claim 1 being independent. Applicants respectfully request reconsideration and withdrawal of the outstanding rejections in light of the amendments and remarks made herein.

The Official Action

In the Office Action dated March 29, 2002, the Examiner objected to claim 1 based on minor informalities. The Examiner further rejected claims 1, 2, 3, and 6 under 35 U.S.C. § 103(a) as being unpatentable over *Furuhashi et al.* (USP 5,909,205); rejected claims 4 and 5 under 35 U.S.C. § 103(a) as being unpatentable over *Furuhashi et al.* in view of *Nally et al.* (USP 5,808,629); rejected claims 7 and 8 under 35 U.S.C. § 103(a) as being unpatentable over *Furuhashi et al.* in view of *Tada et al.* (USP 6,252,563); and rejected claim 9 under 35 U.S.C. § 103(a) as being unpatentable over *Furuhashi et al.* in view of *Selwan* (USP 5,526,025).

Claim Objections

With regard to the Examiner's objection to claim 1 based on minor informalities, by this Amendment, Applicants have amended claim 1 to replace "to/in" with "to". Based upon this amendment, Applicants respectfully request withdrawal of this objection.

Claim Rejections - 35 U.S.C. § 103

With regard to the Examiner's rejection of claims 1, 2, 3, and 6 under 35 U.S.C. § 103(a) as being unpatentable over *Furuhashi et al.*, Applicants respectfully traverse these rejections.

In order to sustain a claim rejection under 35 U.S.C. § 103(a), it is respectfully submitted that the Examiner must meet his burden to establish a *prima facie* case. "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The Examiner asserts *Furuhashi et al.* teaches a frame/line memory control circuit that controls the transfer and storage of the display data from main memory (frame memory 110) to line memory (line memory 111) and the readout of the necessary display data from line memory to display it on the screen.

It is respectfully submitted that *Furuhashi et al.* teaches a liquid crystal display control device. Specifically, *Furuhashi et al.* teaches

> The frame/line memory control circuit 112 serves to control the operation of the frame memory 110 and the line memory 111. Therefore, the frame/line memory control circuit 112 generates the frame memory control signal 113 and the line memory control signal 114 on the basis of the dot clock 106, the synchronous signal 103, the resolution judgment result 108 and a memory access reconciling signal 123, and outputs these signals; to the frame memory 110 and the line memory 111. Further, it outputs a memory architecture decode signal 206 as described later to the display timing generating circuit 120.

> The enlargement processing control circuit 118 performs the enlargement processing by using the frame memory read data 115 and the line memory read data 116, and then outputs the enlargement-processed result as a video signal 119 to the display timing generating circuit 120. The enlargement processing itself by

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the enlargement processing control circuit 118 and the line memory 111 is basically the same as the conventional technique described above.

The display timing generating circuit 120 serves to adjust the timing of each of the video signal 117 and the video signal 119 so as to meet the display timing of the liquid crystal display panel 124. After the timing adjustment, the display timing generating circuit 120 outputs these signals as a video signal 121 to the liquid crystal display panel 124. (Col. 7, line 55 - col. 8, line 12).

In contrast, the present invention as set forth in claim 1 recites, *inter alia*, a programmable display device comprising a display control section which controls the transfer and storage of the display data from the main memory to the line memory and the readout of the necessary display data from the line memory to display it on the screen. It is respectfully submitted that *Furuhashi et al.* fails to teach or suggest a display control section which controls the readout of the necessary display data from the line memory to display it on the screen.

Additionally, the present invention as set forth in claim 1 recites, *inter alia*, a programmable display device comprising the display control section reading out the display data by specifying the address of the display data for one line which has a possibility to be displayed on the screen to the main memory from which the display data is transferred, based upon the stored information, causing the data processing circuit to perform the data transfer and select the line memory to store the display data. It is respectfully submitted that *Furuhashi et al.* fails to teach the display control section of the present invention, and thus claim 1 is patentable over *Furuhashi et al.*

It is respectfully submitted that claims 2-9 are patentable for the reasons set forth above with regard to claim 1 based upon their dependency on claim 1.

CONCLUSION

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number of (703) 205-8000, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH,LLP

By ⟨signature⟩

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CG/CMV/jdm
1152-0237P

Attachment: Version With Markings to Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims have been amended as follows:

1. (Amended) A programmable display device comprising:

a main memory which stores the display data;

a data processing circuit which converts the data format of said display data into the data format of the screen display;

a number of line memories which store the display data converted by said data processing circuit per unit of the display line;

a display control section which controls the transfer and storage of the display data from said main memory [to/in] to said line memory and the readout of the necessary display data from said line memory to display it on the screen; and

a main control section which controls the storage of said display data in said main memory, and the transfer of the stored information including the data format and the storage address to said display control section, wherein

said display control section reading out said display data by specifying the address of the display data for one line which has a possibility to be displayed on the screen to said main memory from which the display data is transferred, based on said stored information, causing said data processing circuit to perform the data transfer and select said line memory to store said display data.